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Bonnie S. Sheridan
Bonnie S. Sheridan

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Ernst et al.

Group Art Unit: Not Assigned

Serial No.: Not Assigned

Examiner: Not Assigned

Filed: Herewith

Docket No.: 1406/48

For: ADDRESS GENERATOR FOR GENERATING ADDRESSES FOR TESTING A CIRCUIT

* *

PRELIMINARY AMENDMENT

Honorable Commissioner for Patents
BOX PATENT APPLICATION
Washington, D.C. 20231

Dear Sir:

Kindly amend the subject application as follows:

IN THE SPECIFICATION:

Please insert the paragraph heading on page 1 of the English translation of the subject application, line 5, as follows:

--Technical Field --.

Please insert the paragraph heading on page 1 of the English translation of the subject application, line 10, as follows:

--Background Art --.

Please insert the paragraph heading on page 3 of the English translation of the subject application, before line 37, as follows:

--Summary of the Invention--.

Please insert the paragraph heading on page 6 of the English translation of the subject application, before line 4, as follows:

--Brief Description of the Drawings--.

Please insert the paragraph heading on page 6 of the English translation of the subject application, before line 23, as follows:

--Detailed Description of the Invention--.

IN THE CLAIMS:

Please delete the paragraph heading on page 15 of the English translation of the subject application, line 1, and insert in place thereof the paragraph heading as follows:

--CLAIMS--

Please insert the paragraph heading on page 15 of the English translation of the subject application, before claim 1, the following:

-- What is claimed is: --.

Please amend claims 1-10 as follows:

1. (Amended) An address generator for generating addresses for testing an addressable circuit, having:

(a) at least one base address register for buffer-storing a base address, the base address register in each case being assigned an associated offset register group having a plurality of offset registers for buffer-storing relative address values;

(b) a first multiplexer circuit, which, in a manner dependent on a base register selection control signal, switches through an address buffer-stored in the base address register to a first input of an addition circuit and to an address bus, which is connected to the circuit to be tested;

(c) a second multiplexer circuit, which, in a manner dependent on the base register selection control signal, through-connects the offset register group associated with the through-connected base address register to a third multiplexer circuit, which, in a manner dependent on an offset register selection control signal, through-connects an offset register of the through-connected offset register group to a second input (61) of the addition circuit;

(d) the addition circuit adding the address present at the first input to the relative address value present at the second input to form an address which is buffer-stored in the base address register.

2. (Amended) The address generator as claimed in claim 1, wherein the base address register and the associated offset registers can be initialized by an external test device, via initialization lines.

3. (Amended) The address generator as claimed in claim 1, wherein the address signal switched through to the address bus can be inverted by a controllable inverting circuit.

4. (Amended) The address generator as claimed in claim 1, wherein the number of offset registers of an offset register group is equal to the number of address test jump variants required for testing the circuit.

5. (Amended) The address generator as claimed in claim 1, wherein the circuit to be tested is a synchronous RAM memory with a high operating clock frequency.

6. (Amended) The address generator as claimed in claim 1, wherein the RAM memory has a multiplicity of memory cells which can be addressed via a multidimensional address space (X, Y).

7. (Amended) The address generator as claimed in claim 1, wherein the number of base address registers corresponds to the dimension (d) of the address space of the memory to be tested.

8. (Amended) The address generator as claimed in claim 1, wherein the base register selection control signals and the offset register selection control signals are applied to the address generator by an external test device via an address control signal bus, the bus width of the address control signal bus being less than the bus width of the address bus of the circuit to be tested.

9. (Amended) The address generator as claimed in claim 1, wherein the line lengths of the address bus lines between the address generator and the circuit to be tested are smaller than the line lengths of the address control lines between the test device and the address generator.

10. (Amended) The address generator as claimed in claim 1, wherein the address generator is integrated in the circuit to be tested.

REMARKS

The amendments to the specification as set forth above are intended to clarify and set apart the various sections of the subject application.

The amendments to the claims as set forth above are intended to remove all multiple dependent claims from the subject application and to more particularly point out and distinctly claim the subject invention.

Attached hereto is a marked-up version of the specification and claims 1-10, which illustrates all of the changes made to the specification and claims pursuant to 37 CFR §1.121. The attached page is captioned "**Version With Markings To Show Changes Made**". Deleted language is bracketed and added language is underlined.

The Commissioner is hereby authorized to charge any deficiencies or credit any overpayments in connection with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS & WILSON, P.A.

Date: 3-6-02

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25297
PATENT TRADEMARK OFFICE

1406/48 REJ/lsg

Serial No.: Not yet assigned

Version With Markings To Show Changes Made

IN THE SPECIFICATION:

The paragraph heading has been inserted on page 1 of the English translation of the subject application, line 5, as follows:

Technical Field

The paragraph heading has been inserted on page 1 of the English translation of the subject application, line 10, as follows:

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Summary of the Invention

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Brief Description of the Drawings

The paragraph heading has been inserted on page 6 of the English translation of the subject application, before line 23, as follows:

Detailed Description of the Invention

IN THE CLAIMS:

The paragraph heading "Patent Claims" on page 15 of the English translation of the subject application has been deleted and the paragraph heading has been inserted in place thereof as follows:

CLAIMS

The paragraph heading has been inserted on page 15 of the English translation of the subject application, before claim 1, as follows:

What is claimed is:

1. (Amended) An address generator for generating addresses for testing an addressable circuit [(2)], having:

(a) at least one base address register [(12)] for buffer-storing a base address, the base address register [(12)] in each case being assigned an associated offset register group [(13)] having a plurality of offset registers for buffer-storing relative address values;

(b) a first multiplexer circuit [(38)], which, in a manner dependent on a base register selection control signal, switches through an address buffer-stored in the base address register [(12)] to a first input [(59)] of an addition circuit [(60)] and to an address bus [(3)], which is connected to the circuit [(2)] to be tested;

(c) a second multiplexer circuit [(17)], which, in a manner dependent on the base register selection control signal, through-connects the offset register group [(13)] associated with the through-connected base address register [(12)] to a third multiplexer circuit [(25)], which, in a manner dependent on an offset register selection control signal, through-connects an offset register of the through-connected offset register group [(13)] to a second input [(61)] of the addition circuit [(60)];

(d) the addition circuit [(60)] adding the address present at the first input to the relative address value present at the second input [(61)] to form an address which is buffer-stored in the base address register [(12)].

2. (Amended) The address generator as claimed in claim 1, [characterized in that] wherein the base address register [(12)] and the associated offset registers [(13)] can be initialized by an external test device [(8)], via initialization lines [(10)].

3. (Amended) The address generator as claimed in claim 1 [or 2, characterized in that], wherein the address signal switched through to the address bus [(3)] can be inverted by a controllable inverting circuit [(54)].

4. (Amended) The address generator as claimed in [one of the preceding claims, characterized in that] claim 1, wherein the number of offset registers of an offset register group [(13)] is equal to the number of address test jump variants required for testing the circuit [(2)].

5. (Amended) The address generator as claimed in [one of the preceding claims, characterized in that] claim 1, wherein the circuit [(2)] to be tested is a synchronous RAM memory with a high operating clock frequency.

6. (Amended) The address generator as claimed in [one of the preceding claims, characterized in that] claim 1, wherein the RAM memory has a multiplicity of memory cells which can be addressed via a multidimensional address space (X, Y).

7. (Amended) The address generator as claimed in [one of the preceding claims, characterized in that] claim 1, wherein the number of base address registers [(12)] corresponds to the dimension (d) of the address space of the memory [(2)] to be tested.

8. (Amended) The address generator as claimed in [one of the preceding claims, characterized in that] claim 1, wherein the base register selection control signals and the offset register selection control signals are applied to the address generator [(1)] by an external test device [(8)] via an address control signal bus [(9)], the bus width of the address control signal bus [(9)] being less than the bus width of the address bus [(3)] of the circuit [(2)] to be tested.

9. (Amended) The address generator as claimed in [one of the preceding claims, characterized in that] claim 1, wherein the line lengths of the address bus lines between the address generator [(1)] and the circuit [(2)] to be tested are smaller than the line lengths of the address control lines between the test device [(8)] and the address generator [(1)].

10. (Amended) The address generator as claimed in [one of the preceding claims, characterized in that] claim 1, wherein the address generator [(1)] is integrated in the circuit [(2)] to be tested.